Joo-Young Kim

School of Electrical Engineering, KAIST, 291 Daehak-ro, Yuseong-gu, Daejeon 34141, South Korea.
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Research Interests

- VLSI Design and Computer Architecture
- AI Accelerators and Domain-Specific Processors
- FPGA & Hardware/Software Co-Design
- Processing-in-Memory & Near Data Processing
- Agile Hardware Development

Education

Ph.D. in Electrical Engineering, KAIST, February 2010
Advisor: Prof. Hoi-Jun Yoo
Dissertation: "High Performance Low Power Real-Time Multi-Object Recognition Processor with Visual Perception Engine"
M.S. in Electrical Engineering and Computer Science, KAIST, February 2007
B.S. in Electrical Engineering, Magna cum Laude, KAIST, February 2005

Employment

- Assistant Professor, KAIST EE (09/2019 – Present)
- Director, AI Semiconductor Systems Research Center (07/20 – Present)
- Senior Hardware Engineering Lead, Microsoft Azure (11/2017 – 08/2019)
- Senior Researcher, Microsoft Research (2/2014 – 10/2017)
- Researcher, Microsoft Research (2/2012 – 1/2014)
- Visiting Researcher, Microsoft Research (9/2010 – 8/2011)
- Post-doctoral Researcher, KAIST (2/2010 – 1/2012)

Honors & Awards

- **2017**: Project Catapult won Geekwire's **Innovation of the Year Award**
- **2016**: "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services" selected for **Communications of the ACM Research Highlights**
- **2016**: "A Cloud-Scale Acceleration Architecture" selected for **IEEE Micro Top Picks** in Computer Architecture
- **2014**: "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services" selected for **IEEE Micro Top Picks** in Computer Architecture
- **2010**: "A Real-time Embedded Vision System with 201.4GOPS 496mW Object Recognition Processor" won **Design Contest Award** at 47th Design Automation Conference (DAC)
- **2008**: "Vision Platform for Mobile Intelligent Robot based on 81.6GOPS Object Recognition Processor" won **Design Contest Award** at 45th Design Automation Conference (DAC)
- **2006**: "A TCAM based Periodic Event Generator for Multi-Node Management in Body Sensor Network" won **Design Contest Award** at 2nd Asian Solid-State Circuits Conference (A-SSCC)

Publications

Refereed Conference Papers

1. Ji-Hoon Kim, Juhyoung Lee, Jinsu Lee, Hoi-Jun Yoo, and **Joo-Young Kim,** "Z-PIM: An Energy-Efficient Sparsity-Aware Processing-In-Memory Architecture with Fully-Variable Weight Precision," *IEEE Symposium*

on VLSI Circuits (VLSI), Jun. 2020

2. Adrian Caulfield, Eric Chung, Andrew Putnam, Hari Angepat, Jeremy Fowers, Michael Haselman, Stephen Heil, Matt Humphrey, Puneet Kaur, **Joo-Young Kim**, Daniel Lo, Todd Massengill, Kalin Ovtcharov, Michael Papamichael, Lisa Woods, Sitaram Lanka, Derek Chiou, and Doug Burger, "A Cloud-Scale Acceleration Architecture," *49th International Symposium on Microarchitecture* (MICRO), Oct. 2016
3. Kalin Ovtcharov, Olatunji Ruwase, **Joo-Young Kim**, Jeremy Fowers, Karin Strauss, Eric Chung, "Toward Accelerating Deep Learning at Scale Using Specialized Logic," *Hot Chips: A Symposium on High Performance Chips* (HOTCHIPS), Aug. 2015
4. Jeremy Fowers, **Joo-Young Kim**, Scott Hauck, and Doug Burger, "A Scalable High-Bandwidth Architecture for Lossless Compression on FPGAs," *23rd International Symposium on Field-Programmable Custom Computing Machines* (FCCM), May 2015
5. Andrew Putnam, Adrian M. Caulfield, Eric S. Chung, Derek Chiou, Kypros Constantinides, John Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, **Joo-Young Kim**, Sitaram Lanka, James R. Larus, Eric Peterson, Gopi Prashanth, Aaron Smith, Jason Thong, Phillip Yi Xiao, and Doug Burger, "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services," *41st International Symposium on Computer Architecture* (ISCA), Jun. 2014
6. Janarbek Matai, **Joo-Young Kim** and Ryan Kastner, "Energy Efficient Canonical Huffman Encoding," *25th International Conference on Application-specific Systems, Architectures and Processors* (ASAP), Jun. 2014
7. **Joo-Young Kim**, Scott Hauck, and Doug Burger, "A Scalable Multi-engine Xpress9 Compressor with Asynchronous Data Transfer," *22nd International Symposium on Field-Programmable Custom Computing Machines* (FCCM), May 2014
8. Seungjin Lee, Jinwook Oh, Minsu Kim, Junyoung Park, Joonsoo Kwon, **Joo-Young Kim**, and Hoi-Jun Yoo, "Intelligent NoC with Neuro-Fuzzy Bandwidth Regulation for a 51 IP Object Recognition Processor," *IEEE Custom Integrated Circuits Conference* (CICC), Sep. 2010
9. Jinwook Oh, Seungjin Lee, Minsu Kim, Joonsoo Kwon, Junyoung Park, **Joo-Young Kim**, and Hoi-Jun Yoo, "A 1.2mW On-Line Learning Mixed Mode Intelligent Inference Engine for Robust Object Recognition," *IEEE Symposium on VLSI Circuits* (VLSI), Jun. 2010
10. Seungjin Lee, Jinwook Oh, Minsu Kim, Joonyoung Park, Joonsoo Kwon, **Joo-Young Kim**, and Hoi-Jun Yoo, "A 36 Heterogeneous Core Architecture with Resource-Aware Fine-grained Task Scheduling for Feedback Attention based Object Recognition," *IEEE Symposium on Low-Power and High-Speed Chips* (COOLCHIPS), Apr. 2010
11. **Joo-Young Kim**, Kwanho Kim, Minsu Kim, Seungjin Lee, Jinwook Oh, and Hoi-Jun Yoo, "A 118.4GB/s Multi-Casting Network-on-Chip for Real-Time Object Recognition Processor," *IEEE European Solid-State Circuits Conference* (ESSCIRC), Sep. 2009
12. **Joo-Young Kim**, Seungjin Lee, Jinwook Oh, Minsu Kim, and Hoi-Jun Yoo, "A 60fps 496mW Multi-Object Recognition Processor with Workload-Aware Dynamic Power Management," *ACM/IEEE International Symposium on Low Power Electronics and Design* (ISLPED), Aug. 2009
13. Minsu Kim, **Joo-Young Kim**, Seungjin Lee, Jinwook Oh, and Hoi-Jun Yoo, "A 22.8GOPS 2.83mW Neuro-fuzzy Object Detection Engine for Fast Multi-Object Recognition," *IEEE Symposium on VLSI Circuits* (VLSI), Jun. 2009
14. **Joo-Young Kim**, Minsu Kim, Seungjin Lee, Jinwook Oh, Kwanho Kim, and Hoi-Jun Yoo, "An Energy Efficient Real-Time Object Recognition Processor with Neuro-Fuzzy Controlled Task Pipelining," *IEEE Symposium on Low- Power and High-Speed Chips* (COOLCHIPS), Apr. 2009
15. **Joo-Young Kim**, Minsu Kim, Seungjin Lee, Jinwook Oh, Kwanho Kim, Sejong Oh, Jeong-Ho Woo, Donghyun Kim, and Hoi-Jun Yoo, "A 201.4GOPS 496mW Real-Time Multi-Object Recognition Processor with Bio-Inspired Neural Perception Engine," *IEEE International Solid-State Circuits Conference* (ISSCC), Feb. 2009
16. **Joo-Young Kim**, Kwanho Kim, Seungjin Lee, Minsu Kim, and Hoi-Jun Yoo, "A 66fps 38mW Nearest Neighbor Matching Processor with Hierarchical VQ Algorithm for Real-Time Object Recognition," *IEEE Asian Solid-State Circuits Conference* (A-SSCC), Nov. 2008
17. Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, Minsu Kim, and Hoi-Jun Yoo, "A 76.8 GB/s 46 mW Low-latency Network-on-Chip for Real-time Object Recognition Processor," *IEEE Asian Solid-State Circuits Conference* (A-SSCC), Nov. 2008

18. Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, Minsu Kim, and Hoi-Jun Yoo, "A 211 GOPS/W Dual-Mode Real-Time Object Recognition Processor with Network-on-Chip," *IEEE European Solid-State Circuits Conference* (ESSCIRC), Sep. 2008
19. Seungjin Lee, Kwanho Kim, Minsu Kim, **Joo-Young Kim**, and Hoi-Jun Yoo, "The Brain Mimicking Visual Attention Engine: An 80x60 Digital Cellular Neural Network for Rapid Global Feature Extraction," *IEEE Symposium on VLSI Circuits* (VLSI), Jun. 2008
20. Donghyun Kim, Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, and Hoi-Jun Yoo, "Vision Platform for Mobile Intelligent Robots Based on 81.6 GOPS Objects Recognition Processor," *ACM Design Automation Conference* (DAC), Jun. 2008
21. Joonsung Bae, **Joo-Young Kim**, and Hoi-Jun Yoo, "A 0.6pJ/b 3Gb/s/ch Transceiver in 0.18 um CMOS for 10mm On-chip interconnects," *IEEE International Symposium on Circuit and Systems* (ISCAS), May 2008
22. Kwanho Kim, Seungjin Lee, **Joo-Young Kim**, Minsu Kim, Donghyun Kim, Jeong-Ho Woo, and Hoi-Jun Yoo, "A 125GOPS 583mW Network-on-Chip Based Parallel Processor with Bio-inspired Visual Attention Engine," *IEEE International Solid-State Circuits Conference* (ISSCC), Feb. 2008
23. **Joo-Young Kim**, and Hoi-Jun Yoo, "Bitwise Competition Logic for Compact Digital Comparator," *IEEE Asian Solid-State Circuits Conference* (A-SSCC), Nov. 2007
24. Donghyun Kim, Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, and Hoi-Jun Yoo, "Implementation of Memory-Centric NoC for 81.6 GOPS Object Recognition Processor," *IEEE Asian Solid-State Circuits Conference* (A-SSCC), Nov. 2007
25. **Joo-Young Kim**, Donghyun Kim, Seungjin Lee, Kwanho Kim, and Hoi-Jun Yoo, "Visual Image Processing RAM for Fast 2-D Data Location Search," *IEEE European Solid-State Circuits Conference* (ESSCIRC), Sep. 2007
26. Donghyun Kim, Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, and Hoi-Jun Yoo, "An 81.6 GOPS Object Recognition Processor Based on NoC and Visual Image Processing Memory," *IEEE Custom Circuits Conference* (CICC), Sep. 2007
27. Donghyun Kim, Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, and Hoi-Jun Yoo, "Solutions for Real Chip Implementation Issues of NoC and Their Application to Memory-Centric NoC," *IEEE International Symposium on Network-on-Chip* (NOCS), May 2007
28. **Joo-Young Kim**, Kangmin Lee, and Hoi-Jun Yoo, "A 372ps 64-bit Adder using Fast Pull-up Logic in 0.18-um CMOS," *IEEE International Symposium on Circuit and Systems* (ISCAS), May 2006
29. Sungdae Choi, Kyomin Sohn, **Jooyoung Kim**, Jerald Yoo, and Hoi-Jun Yoo, "A TCAM-based Periodic Event Generator for Multi-Node Management in the Body Sensor Network," *IEEE Asian Solid-State Circuits Conference* (A-SSCC), Nov. 2006
30. Kyomin Sohn, Sungdae Choi, Jeong-Ho Woo, **Jooyoung Kim**, and Hoi-Jun Yoo, "A 0.6-V, 6.8-uW Embedded SRAM for Ultra-low Power SoC," *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2006
31. Sungdae Choi, Seong-Jun Song, Kyomin Sohn, Hyejung Kim, **Jooyoung Kim**, Namjun Cho, Jeong-Ho Woo, Jerald Yoo and Hoi-Jun Yoo, "A 24.2-uW Dual-Mode Human Body Communication Controller for Body Sensor Network," *IEEE European Solid-State Circuits Conference* (ESSCIRC), Sep. 2006
32. Sungdae Choi, Seong-Jun Song, Kyomin Sohn, Hyejung Kim, **Jooyoung Kim**, Namjun Cho, Jeong-Ho Woo, Jerald Yoo and Hoi-Jun Yoo, "A Multi-Nodes Human Body Communication Sensor Network Control Processor," *IEEE Custom Circuits Conference* (CICC), Sep. 2006
33. Sungdae Choi, Seong-Jun Song, Kyomin Sohn, Hyejung Kim, **Jooyoung Kim**, Jerald Yoo, and Hoi-Jun Yoo, "A Low-power Star-topology Body Area Network Controller for Periodic Data Monitoring Around and Inside the Human Body," *IEEE International Symposium on Wearable Computers* (ISWC), Jun. 2006

Journal Papers

34. Ji-Hoon Kim, Juhyung Lee, Jinsu Lee, Jaehoon Heo, and **Joo-Young Kim**, "Z-PIM: A Sparsity-Aware Processing-In-Memory Architecture with Fully-Variable Weight Bit-Precision for Energy-Efficient Deep Neural Networks," Accepted at *IEEE Journal of Solid-State Circuits* (JSSC), 2021
35. Ji-Hoon Kim, Changhyeon Kim, Kwantae Kim, Juhyung Lee, Hoi-Jun Yoo, and **Joo-Young Kim**, "An Ultra-low-power Mixed-mode Face Recognition Processor for Always-on User Authentication in Mobile Device," *Journal of Semiconductor Technology and Science* (JSTS), Vol. 20, No. 6, Dec. 2020

36. Adrian Caulfield, Eric Chung, Andrew Putnam, Hari Angepat, Daniel Firestone, Jeremy Fowers, Michael Haselman, Stephen Heil, Matt Humphrey, Puneet Kaur, **Joo-Young Kim**, Daniel Lo, Todd Massengill, Kalin Ovtcharov, Michael Papamichael, Lisa Woods, Sitaram Lanka, Derek Chiou, Doug Burger, "Configurable Clouds," *IEEE Micro*, Vol. 37, No. 3, May/Jun. 2017
37. Andrew Putnam, Adrian Caulfield, Eric Chung, Derek Chiou, Kypros Constantinides, John Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Gopi Prashanth Gopal, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, **Joo-Young Kim**, Sitaram Lanka, James Larus, Eric Peterson, Simon Pope, Aaron Smith, Jason Thong, Phillip Yi Xiao, Doug Burger, "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services," *Communications of the ACM*, Vol. 59, No. 11, Nov. 2016
38. Andrew Putnam, Adrian M. Caulfield, Eric S. Chung, Derek Chiou, Kypros Constantinides, John Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, **Joo-Young Kim**, Sitaram Lanka, James R. Larus, Eric Peterson, Gopi Prashanth, Aaron Smith, Jason Thong, Phillip Yi Xiao, and Doug Burger, "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services," *IEEE Micro*, May 2015
39. Kalin Ovtcharov, Olatunji Ruwase, **Joo-Young Kim**, Jeremy Fowers, Karin Strauss, and Eric S. Chung, "Accelerating Deep Convolutional Neural Networks Using Specialized Hardware," *Microsoft White paper*, Feb. 2015
40. Jinwook Oh, Gyeonghoon Kim, Junyoung Park, Injoon Hong, Seungjin Lee, **Joo-Young Kim**, Jeong-Ho Woo, and Hoi-Jun Yoo, "A 320mW 342GOPS Real-Time Dynamic Object Recognition Processor for HD 720p Video Streams," *IEEE Journal of Solid-State Circuits* (JSSC), Vol. 48, No. 1, Jan. 2013
41. Jinwook Oh, Gyeonghoon Kim, Junyoung Park, Injoon Hong, Seungjin Lee, **Joo-Young Kim**, Jeong-Ho Woo, and Hoi-Jun Yoo, "Low-Power, Real-Time Object Recognition Processor for Mobile Vision Systems," *IEEE Micro*, Vol. 32, No. 6, Nov./Dec. 2012
42. Junyoung Park, Joonsoo Kwon, Jinwook Oh, Seungjin Lee, **Joo-Young Kim**, and Hoi-Jun Yoo, "A 92mW Real-Time Traffic Sign Recognition System with Robust Illumination Adaptation and Support Vector Machine," *IEEE Journal of Solid-State Circuits* (JSSC), Vol. 47, No. 11, Nov. 2012
43. Seungjin Lee, Minsu Kim, Kwanho Kim, **Joo-Young Kim**, and Hoi-Jun Yoo, "24-GOPS 4.5-mm2 Digital Cellular Neural Network for Rapid Visual Attention in an Object-Recognition SoC," *IEEE Transactions on Neural Networks*, Vol. 22, No. 1, Jan. 2011
44. **Joo-Young Kim**, Junyoung Park, Seungjin Lee, Minsu Kim, Jinwook Oh, and Hoi-Jun Yoo, "A 118.4GB/s Multi-Casting Network-on-Chip with Hierarchical Star-Ring Combined Topology for Real-Time Object Recognition," *IEEE Journal of Solid-State Circuits* (JSSC), Vol. 45, No. 7, Jul. 2010
45. **Joo-Young Kim**, Sejong Oh, Seungjin Lee, Minsu Kim, Jinwook Oh, and Hoi-Jun Yoo, "An Attention Controlled Multi-Core Architecture for Energy Efficient Object Recognition," *Elsevier Signal Processing: Image Communication*, Vol. 25, No. 5, Jun. 2010
46. **Joo-Young Kim**, Donghyun Kim, Kwanho Kim, Seungjin Lee, and Hoi-Jun Yoo, "Visual Image Processing RAM: Memory Architecture with 2-D Data Location Search and Data Consistency Management for a Multi-Core Object Recognition Processor," *IEEE Transactions on Circuits and Systems for Video Technology*, Vol. 20, No. 4, Apr. 2010
47. Seungjin Lee, Kwanho Kim, **Joo-Young Kim**, Minsu Kim, and Hoi-Jun Yoo, "Familiarity Based Unified Visual Attention Model for Fast and Robust Object Recognition," *Elsevier Pattern Recognition*, Vol. 43, No. 3, Mar. 2010
48. **Joo-Young Kim**, Minsu Kim, Seungjin Lee, Jinwook Oh, Kwanho Kim and Hoi-Jun Yoo, "A 201.4GOPS 496mW Real-Time Multi-Object Recognition Processor with Bio-Inspired Neural Perception Engine," *IEEE Journal of Solid-State Circuits* (JSSC), Vol. 45, No. 1, Jan. 2010
49. **Joo-Young Kim**, Minsu Kim, Seungjin Lee, Jinwook Oh, Sejong Oh, and Hoi-Jun Yoo, "Real-Time Object Recognition with Neuro-Fuzzy Controlled Workload-aware Task Pipelining," *IEEE Micro*, Vol. 29, No. 6, Nov./Dec. 2009
50. Kwanho Kim, Seungjin Lee, **Joo-Young Kim**, Minsu Kim, and Hoi-Jun Yoo, "A Configurable Heterogeneous Multicore Architecture with Cellular Neural Network for Real-Time Object Recognition," *IEEE Transactions on Circuits and Systems for Video Technology*, Vol. 19, No. 11, Nov. 2009
51. Donghyun Kim, Kwanho Kim, Seungjin Lee, **Joo-Young Kim**, Minsu Kim, and Hoi-Jun Yoo, "Memory-

Centric Network-on-Chip for Power Efficient Execution of Task-Level Pipeline on a Multi-Core Processor," *IET Computers & Digital Techniques*, Vol. 3, No. 5, Sep. 2009

52. Donghyun Kim, Kwanho Kim, **Joo-Young Kim**, Seungjin Lee, Se-Joong Lee, and Hoi-Jun Yoo, "81.6 GOPS Object Recognition Processor Based on a Memory-Centric NoC," *IEEE Transactions on Very Large Scale Integration*, Vol. 17, No. 3, Mar. 2009
53. Kwanho Kim, Seungjin Lee, **Joo-Young Kim**, Minsu Kim, and Hoi-Jun Yoo, "A 125 GOPS 583 mW Network-on-Chip Based Parallel Processor with Bio-Inspired Visual Attention Engine," *IEEE Journal of Solid-State Circuits* (JSSC), Vol. 44, No. 1, Jan. 2009

Patents

54. **Joo-Young Kim**, Doug Burger, Jeremy Fowers, and Scott Hauck, "Scalable High-Bandwidth Architecture for Lossless Compression," U.S. Patent 9,590,655, Issued on Mar. 7, 2017
55. Eric Chung, Karin Strauss, Kalin Ovtcharov, **Joo-Young Kim**, and Olatunji Ruwase, "Deep Neural network partitioning on servers," U.S. Patent App. 14/754,384
56. Eric Chung, Karin Strauss, Kalin Ovtcharov, **Joo-Young Kim**, and Olatunji Ruwase, "Convolutional neural networks on hardware accelerators," US Patent App. 14/754,367
57. Minsu Kim, **Joo-Young Kim**, and Hoi-Jun Yoo, "Binary Number Comparator," Korean Patent No.10-10916840000, Issued on Nov. 2, 2011
58. **Joo-Young Kim** and Hoi-Jun Yoo, "Network on Chip and Network on Chip Systems," Korean Patent No.10-10775390000, Issued on Oct. 21, 2011
59. Jinwook Oh, **Joo-Young Kim**, and Hoi-Jun Yoo, "Computer System Combining Neuro-Fuzzy System and Parallel Processor and Objects Recognizing System using Thereof," Korean Patent No.10-10696020000, Issued on Sep. 27, 2011
60. **Joo-Young Kim** and Hoi-Jun Yoo, "Multi Casting Network on Chip, Systems Thereof and Network Switch," Korean Patent No.10-10334250000, Issued on Apr. 29, 2011
61. **Joo-Young Kim** and Hoi-Jun Yoo, "Method and Apparatus for Recognizing Objects in an Image," Korean Patent No.10-10279060000, Issued on Apr. 1, 2011
62. Minsu Kim, **Joo-Young Kim**, and Hoi-Jun Yoo, "Apparatus and Method for Detecting a Plurality of Objects In an Image," Korean Patent No.10-10182990000, Feb. 22, 2011
63. **Joo-Young Kim** and Hoi-Jun Yoo, "Apparatus and Method Transmitting-Receiving Data," Korean Patent No.10-09461770000, Issued on Mar. 2, 2010
64. **Joo-Young Kim** and Hoi-Jun Yoo, "High Speed Serializing-Deserializing System and Method," Korean Patent No.10-09364450000, Issued on Jan. 5, 2010
65. **Joo-Young Kim** and Hoi-Jun Yoo, "Arithmetic Apparatus of Microprocessor," Korean Patent No.10-09188150000, Issued on Aug. 17, 2009

Teaching

- EE878 Hardware Acceleration for Machine Learning, Spring 2020
- EE303 Digital System Design, Fall 2019/2020

Grants

Government Agencies

- Principal Investigator, IITP, "Development of Semiconductor/Systems-Integrated Technologies for Remote/AI based Society," 07/2020-12/2025, 912,700,000 KRW/year
- Principal Investigator, NRF, "Research and Development on SIMD Extension for Supercomputer CPU," 07/2020-04/2024, 100,000,000 KRW/year
- Co-PI, ADD, "Development of Global Indoor Positioning System for Warrior Platform," 12/2020-12/2022, 194,180,000 KRW/year
- Principal Investigator, KAIST, "High Performance AI Processor Architecture with Processing-in-Memory," 09/2019-12/2022, 200,000,000 KRW

Samsung Electronics

- Principal Investigator, Samsung Electronics, "A Scalable Computation Storage Platform for Data-Intensive Applications," 09/2020-08/2025, 70,000,000 KRW/year
- Principal Investigator, Samsung Electronics, "Non-Von-Neumann Architecture," 09/2019-04/2021, 200,000,000 KRW

SK Hynix

- Principal Investigator, SK Hynix, "FPGA based DNN Accelerators," 06/2020-11/2021, 50,000,000 KRW
- Co-PI, SK Hynix, "ML Accelerator and Platform," 02/2020-11/2021, 100,000,000 KRW

Professional Activities

Conference and Professional Society Organization

- Publication Co-Chair, International Conference on Artificial Intelligence Circuits and Systems (AICAS), 2020
- Technical Committee Chair, KAIST EE-CS joint workshop, January 2012
- Technical Committee Chair, KAIST-Keio-Tsinghua (KKT) workshop, August 2009

Technical Program Committee

- ACM/IEEE Design Automation Conference (DAC), 2020-2021
- IEEE Asian Solid-State Circuits Conference (A-SSCC), 2021
- IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2021
- International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART), 2014-2019

Journal Editing

- Associate Editor, IEEE Transactions on Circuits and Systems- I (TCAS-I), 2020-2021
- Guest Editor, MDPI Electronics Special Issue, "Advanced AI Hardware Designs Based on FPGAs", 2020

Invited Talks / Tutorials

1. Tutorial: "AI Accelerators for Cloud Datacenters," IEEE International SoC Conference (ISOCC), Yeosu, South Korea, Oct. 2020
2. Invited Talk: "AI Chip Trends and Forecast," ICT Industry Outlook Conference, Seoul, South Korea, Nov. 2019
3. Invited Talk: "Hardware Acceleration for Cloud Datacenters," KAIST, Daejeon, South Korea, Nov. 2018
4. Tutorial: "Accelerating Deep Convolutional Neural Networks Using Specialized Hardware in the Datacenter," IEEE Asian Solid-State Circuits Conference (A-SSCC), Toyama, Japan, Nov. 2016
5. Invited Talk: "Accelerating Deep Convolutional Neural Networks Using Specialized Hardware in the Datacenter," Deep Neural SoC Workshop, KAIST, Daejeon, South Korea, Aug. 2016
6. Invited Talk: "Accelerating Deep Convolutional Neural Networks Using Specialized Hardware in the Datacenter," Samsung Advanced Institute of Technology (SAIT), Suwon, South Korea, Aug. 2016
7. Invited Talk: "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services," Naver Labs, Seongnam, South Korea, Apr. 2015
8. Invited Talk: "Hardware Accelerators on FPGA," Northwest Regional Conference, Seattle, WA, Sep. 2013
9. Invited Talk: "Robust 6-DOF Camera Tracking for Mobile Augmented Reality", Chungnam National University, Daejeon, South Korea, Dec. 2011
10. Invited Talk: "High Performance Low Power Real-Time Multi-Object Recognition Processor with Visual Perception Engine," Intel/Nvidia/Texas Instruments/IMEC/ Technical University of Eindhoven, Aug./Sep. 2009

External Reviewer

Served as an external reviewer for various conference and journal papers including IEEE JSSC, IEEE ISSCC, IEEE TCAS-I, IEEE TCAS-II, IEEE VLSI, IEEE A-SSCC, ACM/IEEE NOCS, IEEE ISCAS.

Intern Supervision

David Ojika, University of Florida
Ming Liu, Massachusetts Institute of Technology
Peipei Zhou, University of California Los Angeles
Janarbek Matai, University of California San Diego
Jinwook Oh, Korea Advanced Institute of Science and Technology

Personal

Citizen of South Korea. Permanent resident of United States.